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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,208	10/08/2003	Alan J.A. Trainor	115-34US/12667/100119	7464

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EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/680,208	TRAINOR, ALAN J.A.	
	Examiner	Art Unit	
	STANETTA D. ISAAC	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 April 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/25/08 & 4/28/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response the amendment filed on 4/28/08. Currently, claims 1-26 are pending. Claims 8, 13, 14, 20, 21, and 25 are withdrawn from further consideration.

Examiner's Remarks

The Examiner has taken the Applicant's remarks filed on 4/28/08 into further consideration regarding the election/restriction requirement mailed in the Office Action 12/26/07. The Examiner finds the Applicant's arguments persuasive and as a result, has rejoined claims 3, 4, 8, 13, 14, 20, 21 and 25 on the merits.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 5, 6, 7, 9-12,15-19, 22-24 and 26, are rejected under 35 U.S.C. 102(b) as being anticipated by Kitsukawa et al., US Patent 5,844,853.

3. Kitsukawa discloses the semiconductor apparatus as claimed. See figures 1a-18, and corresponding text where, Kitsukawa teaches pertaining to claims 1 and 17, an electronic apparatus comprising: a first integrated circuit semiconductor die **8a** comprising: a first signal conditioning circuit integrated within the first integrated circuit die for performing a first signal conditioning function on a signal propagating along a first signal path (figure 3a; col. 3, lines 55-

67); a first ancillary circuit integrated **22** within the first integrated circuit die and electrically coupled to the first signal conditioning circuit for other than performing the first signal conditioning function and for use by the first signal conditioning circuit during operation thereof (figure 3a; col. 4, lines 1-7); a second integrated circuit semiconductor die **8b** comprising a second signal conditioning circuit integrated within the second integrated circuit die for performing a second signal conditioning function on a signal propagating along a second signal path that is different than the first signal path (figure 3b; col. 3, lines 55-67; col. 4, lines 1-7); a second ancillary circuit integrated **24** within the first integrated circuit semiconductor die and electrically coupled to the second signal conditioning circuit for other than performing the second signal conditioning function and for use by the second signal conditioning circuit during operation thereof (figures 3a and 3b; col. 3, lines 55-67; col. 4, lines 1-8); a substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies (figure 2a; col. 3, lines 30-55).

4. Kitsukawa teaches, pertaining to claim 2, wherein the first signal conditioning function and the second signal conditioning function provide similar signal conditioning operations (col. 4, lines 1-7).

5. Kitsukawa teaches, pertaining to claim 5, wherein the first signal conditioning circuit comprises at least a power amplifier circuit and where the function of the first signal conditioning circuit is for amplifying of an input signal using the at least a power amplifier circuit.

6. Kitsukawa teaches, pertaining to claim 6, wherein the second signal conditioning circuit comprises at least a power amplifier circuit and where the function of the second signal conditioning circuit is for amplifying of an input signal using the at least a power amplifier circuit.

7. Kitsukawa teaches, pertaining to claim 7, wherein the second semiconductor process does not facilitate manufacturing and integration of the second ancillary circuit therein (figure 3a-3b).

8. Kitsukawa teaches, pertaining to claim 9, wherein the first ancillary circuit comprises at least one of voltage regulation circuitry and temperature control circuitry (figures 3a and 3b; col. 4, lines 1-7).

9. Kitsukawa teaches pertaining to claim 10, wherein the second ancillary circuit comprises at least one of voltage regulation circuitry and temperature control circuitry (col. 4, lines 7-25).

10. Kitsukawa teaches, pertaining to claim 11, wherein the first integrated circuit die is derived from a first semiconductor wafer comprised of one of Si, SiGe, GaAs, InP, and GaN. (col. 1, lines 15-17)

11. Kitsukawa teaches pertaining to claim 12, wherein the second integrated circuit die is derived from a second semiconductor wafer the other one of Si, SiGe, GaAs, InP, and GaN (col. 1, lines 15-17).

12. Kitsukawa teaches, pertaining to claim 15, wherein the first integrated circuit die comprises a first interface port connected to the second ancillary circuit and wherein the second integrated circuit die comprises a second interface port connected to the second signal conditioning circuit, the second signal conditioning circuit for being connected to the second ancillary circuit using the first and second interface ports (figure 3a and 3b).

13. Kitsukawa teaches, pertaining to claim 16, wherein the second signal conditioning circuit is for performing the second signal conditioning function in conjunction with operation of the second ancillary circuit (figures 3a and 3b).

14. Kitsukawa teaches, pertaining to claim 18, wherein the second integrated circuit die cannot provide the second function without operation of the second ancillary circuit (figure 3a and 3b; col. 4, lines 1-25)

15. Kitsukawa teaches, pertaining to claim 19, wherein the first signal conditioning function and the second signal conditioning function provide similar signal conditioning operations (figures 3a and 3b).

16. Kitsukawa teaches, pertaining to claim 22, wherein at least one of the first signal conditioning circuit and the second signal conditioning circuit comprises at least a power amplifier circuit. (figure 12; col. 7, lines 62-67l col. 8, lines 1-11)

17. Kitsukawa teaches, pertaining to claim 23, wherein the first ancillary circuit and the second ancillary circuit each comprises at least one of voltage regulation circuitry and temperature control circuitry (col. 4, lines 1-7).

18. Kitsukawa teaches, pertaining to claim 24, wherein the first integrated circuit die is derived from a first semiconductor wafer comprised of one of Si, SiGe, GaAs, InP, and GaN (col. 1, lines 15-17).

19. Kitsukawa teaches, pertaining to claim 26, comprising a module substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies (col. 4, lines 1-7).

20. Claims 3, 4, 8, 13, 14, 20, 21, and 25 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kitsukawa et al., US Patent 5,844,853.

21. Kitsukawa discloses the semiconductor device substantially as claimed. Please see above rejection.

22. However, Kitsukawa fails to show, pertaining to claims 3 and 20, wherein the first integrated circuit die is manufactured using a first semiconductor process and utilizes a silicon based technology. In addition, Kitsukawa fails to show, pertaining to claims 4 and 21, wherein the second integrated circuit die is manufactured using a second semiconductor process and utilizes an other than silicon based technology. Also, Kitsukawa fails to show, pertaining to claim 8, wherein the first integrated circuit die is manufactured using a first semiconductor process and utilizes a first semiconductor technology and the second integrated circuit die is manufactured using a second semiconductor process and utilizes a second semiconductor based technology. Kitsukawa fails to show pertaining to claims 13 and 25, wherein the first integrated circuit die is manufactured using a first semiconductor process and utilizes a BiCMOS based technology. Finally, Kitsukawa fails to show, pertaining to claim 14, wherein the first integrated circuit die is derived from a first semiconductor wafer comprised of SiGe.

23. Kitsukawa teaches an electronic apparatus that includes first and second integrated circuit semiconductor dies.

24. It would have been obvious to one of ordinary skill in the art to incorporate the following steps of: wherein the first integrated circuit die is manufactured using a first semiconductor process and utilizes a silicon based technology; wherein the second integrated circuit die is

manufactured using a second semiconductor process and utilizes an other than silicon based technology; wherein the first integrated circuit die is manufactured using a first semiconductor process and utilizes a first semiconductor technology and the second integrated circuit die is manufactured using a second semiconductor process and utilizes a second semiconductor based technology; wherein the first integrated circuit die is manufactured using a first semiconductor process and utilizes a BiCMOS based technology; wherein the first integrated circuit die is derived from a first semiconductor wafer comprised of SiGe, in the electronic apparatus of Kitsukawa, pertaining to claims 3, 4, 8, 13, 14, 20, 21 and 25, according to the teachings of Kitsukawa, with the motivation that Kitsukawa teaches the final electronic apparatus where the apparatus containing the first and second integrated semiconductor dies can be made by conventionally known semiconductor processing in the art, since the patentability of the process must not be determined in the electronic apparatus.(see *In re Taylor*, 149 USPQ 615, 617 (CCPA 1966) and *In re Thorpe*, 227 USPQ 964,966 (CAFC 1985), *Ex parte Edwards* 231 USPQ 981, 983, (BdPatApp&Int 1986)).

Response to Arguments

25. Applicant's arguments filed 4/28/08 have been fully considered but they are not persuasive. In the Remarks on pages 11-12:

26. The Applicant raises the clear issue as to whether Kitsukawa teaches a first and second integrated circuit dies.

27. The Examiner takes the position that Kitsukawa does teach first and second integrated circuit dies. Specifically, Kitsukawa teaches a 256 Mbit DRAM that includes a 3.3V *device* **8a** and a 2.5V *device* **8b** (see figures 3a and 3b; col. 3, lines 55-67).

28. Applicant's arguments with respect to claims 3, 4, 8, 13, 14, 20, 21 and 25 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STANETTA D. ISAAC whose telephone number is (571)272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stanetta Isaac
Patent Examiner
October 21, 2008

/Charles D. Garber/
Supervisory Patent Examiner, Art Unit 2812